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Sheet 1 of 1

Complete if Known

Application Number	10/602,020
Filing Date	June 24, 2003
First Named Inventor	Frederic Reblewski
Art Unit	2123-2128
Examiner Name	TBA
Attorney Docket Number	003921.00135

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
A		US- 6,473,726	10-29-2002	Reblewski	
		US-6,265,894	07-24-2001	Reblewski et al.	
		US- 6,184,707	02-06-2001	Norman et al.	
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		US- 5,777,489	07-07-1998	Barbier et al.	
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		US- 5,036,473	07-30-1991	Butts et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
A		WO 94/06210	03-17-1994	Prabhakar Goel		
		EP 0 651 343	05-03-95	Quickturn Systems, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
A		CHARLES CLOS, "A Study of Non-Blocking Switching Networks", The Bell System Technical Journal, March 1953, pages 406-424	
		WERNER ERHARD et al., "First Steps towards a Reconfigurable Asynchronous System", Friedrich-Schiller University Jena, Department of Computer Science, IEEE International Workshop on Rapid System Prototyping, June 1999, pages 28-31	
		FATIH KOCAN et al., "Concurrent D-Algorithm on Reconfigurable Hardware", IEEE 1999, pages 152-155	
		JACK JEAN et al., "Dynamic Reconfiguration to Support Concurrent Applications", IEEE Transactions Of Computers, Vol. 48, No. 6, June 1999, pages 591-602	
		BERNARD BOSI et al., "Reconfigurable Pipelined 2-D Convolvers for Fast Digital Signal Processing", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, No. 3, September 1999, pages 299-308	
		A. EJNIOUI et al., "Design Partitioning on Single-Chip Emulation Systems", Center for Microelectronics Research, Dept. of CSE, University of South Florida, 13 th International Conference on VLSI Design, 2000, pages 234-239	
		GREG SNIDER, "The Teramac Compiler", Hewlett-Packard, 1998, pages 1-51	
A		Xilinx, "Programmable Gate Array Design Handbook", First Edition, 1988, pages I-A10	
		JONATHAN BABB, et al., "Logic Emulation with Virtual Wires", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pages 1-20	

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1/9/06

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